DIGITAL ELECTRONICS MCQs

1. A 8-bit serial in / parallel out shift register contains the value "8", _____ clock signal(s) will be required to shift the value completely out of the register.

A. 1 B. 2 C. 4 **D. 8**

Ans.: D

2. In a sequential circuit the next state is determined by _____ and _____.

A. State variable, current state B. Current state, flip-flop output

C. **Current state and external input** D. Input and clock signal applied

Ans.: C

3. The divide-by-60 counter in digital clock is implemented by using two cascading counters:

A. Mod-6, Mod-10 B. Mod-50, Mod-10 C. Mod-10, Mod-50 D. Mod-50, Mod-6

Ans.: A

4. The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.

A. Set-up time **B. Hold time**

C. Pulse Interval time D. Pulse Stability time (PST)

Ans.: B

5. _____ is said to occur when multiple internal variables change due to change in one input variable.

A. Clock Skew **B. Race condition** C. Hold delay D. Hold and Wait

Ans.: B

6. The _____ input overrides the _____ input.

A. Asynchronous, synchronous B. Synchronous, asynchronous

C. Preset input (PRE), Clear input (CLR) D. Clear input (CLR), Preset input (PRE)

Ans.: A

7. A decade counter is _____.

A. Mod-3 counter B. Mod-5 counter C. Mod-8 counter **D. Mod-10 counter**

Ans.: D

8. In asynchronous transmission when the transmission line is idle, _____.

A. It is set to logic low **B. It is set to logic high**

C. Remains in previous state D. State of transmission line is not used to start transmission

Ans.: B

9. A Nibble consists of _____ bits.

A. 2 **B. 4** C. 8 D. 16

Ans.: B

10. The voltage gain of the Inverting Amplifier is given by the relation _____ .

A. Vout / Vin = - Rf / Ri B. Vout / Rf = - Vin / Ri

C. Rf / Vin = - Ri / Vout D. Rf / Vin = Ri / Vout

Ans.: A

11. LUT is acronym for _____ .

A. Look Up Table B. Local User Terminal

C. Least Upper Time Period D. None of given options

Ans.: A

12. The three fundamental gates are _____.

A. AND, NAND, XOR B. OR, AND, NAND

C. NOT, NOR, XOR **D. NOT, OR, AND**

Ans.: D

13. The total amount of memory that is supported by any digital system depends upon _____. A. The organization of memory B. The structure of memory

C. The size of decoding unit **D. The size of the address bus of the microprocessor**

Ans.: D

14. Stack is an acronym for _____ .

A FIFO memory **B. LIFO memory**

C. Flash Memory D. Bust Flash Memory

Ans.: B

15. _____ is one of the examples of synchronous inputs.

A. J-K input B. EN input C. Preset input (PRE) D. Clear Input (CLR)

Ans.: A

16. In a state diagram, the transition from a current state to the next state is determined by:

A. Current state and the inputs B. Current state and outputs

C. Previous state and inputs D. Previous state and outputs

Ans.: A

17. _____ is used to simplify the circuit that determines the next state.

A. State diagram B. Next state table C. State reduction **D. State assignment**

Ans.: D

18. A 8-bit serial in / parallel out shift register contains the value “8”, _____ clock signal(s) will be required to shift the value completely out of the register.

A. 1 B. 2 C. 4 **D. 8**

Ans.: D

19. The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____.

A. Doesn’t have an invalid state

B. Sets to clear when both J = 0 and K = 0

C. It does not show transition on change in pulse

D. It does not accept asynchronous inputs

Ans.: A

20. A positive edge-triggered flip-flop changes its state when _____ .

A. Low-to-high transition of clock B. High-to-low transition of clock
C. Enable input (EN) is set D. Preset input (PRE) is set
Ans.: A

21. In a sequential circuit the next state is determined by _____ and _____.
A. State variable, current state B. Current state, flip-flop output
C. Current state and external input **D. Input and clock signal applied**
Ans.: D

22. The divide-by-60 counter in digital clock is implemented by using two cascading counters: **A. Mod-6, Mod-10** B. Mod-50, Mod-10
C. Mod-10, Mod-50 D. Mod-50, Mod-6
Ans.: A

23. Flip flops are also called _____.
A. Bi-stable dualvibrators B. Bi-stable transformer
C. Bi-stable multivibrators D. Bi-stable singlevibrators
Ans.: C

24. The minimum time for which the input signal has to be maintained at the input of flip-flop is called _____ of the flip-flop.
A. Set-up time **B. Hold time**
C. Pulse Interval time D. Pulse Stability time (PST)
Ans.: B

25. A decade counter is _____.
A. Mod-3 counter B. Mod-5 counter
C. Mod-8 counter **D. Mod-10 counter**
Ans.: D

26. DRAM stands for _____.
A. Dynamic RAM B. Data RAM C. Demoduler RAM D. None of above
Ans.: A

27. The expression F=A+B+C describes the operation of three bits _____ Gate.
A. OR B. AND C. NOT D. NAND
Ans.: A

28. The decimal “17” in BCD will be represented as _____.
A. 11101 B. 11011 **C. 10111** D. 11110
Ans.: C

29. The basic building block for a logical circuit is _____.
A. A Flip-Flop **B. A Logical Gate** C. An Adder D. None of above
Ans.: B

30. The output of the expression F=A.B.C will be Logic _____ when A=1, B=0, C=1.
A. Undefined B. One **C. Zero** D. No Output as input is invalid

Ans.: C

31. _____ is invalid number of cells in a single group formed by the adjacent cells in K-map. A. 2 B. 8 **C. 12** D. 16

Ans.: C

32. _____ is one of the examples of asynchronous inputs.

A. J-K input B. S-R input C. D input **D. Clear Input (CLR)**

Ans.: D

33. 5-bit Johnson counter sequences through ____ states.

A. 7 **B. 10** C. 32 D. 25

Ans.: B

34. FIFO is an acronym for _____.

A. First In, First Out B. Fly in, Fly Out

C. Fast in, Fast Out D. None of given options

Ans.: A

35. _____ of a D/A converter is determined by comparing the actual output of a D/A converter with the expected output.

A. Resolution **B. Accuracy** C. Quantization D. Missing Code

Ans.: B

36. The sequence of states that are implemented by a n-bit Johnson counter is:

A. n+2 (n plus 2) **B. 2n (n multiplied by 2)**

C. 2n (2 raise to power n) D. n2 (n raise to power 2)

Ans.: B

37. "A + B = B + A" is _____.

A. Demorgan□s Law B. Distributive Law

C. Commutative Law D. Associative Law

Ans.: C

38. Demultiplexer is also called:

A. Data selector B. Data router **C. Data distributor** D. Data encoder

Ans.: C

39. The operation of J-K flip-flop is similar to that of the SR flip-flop except that the J-K flip-flop _____.

A. Doesn't have an invalid state

B. Sets to clear when both J = 0 and K = 0

C. It does not show transition on change in pulse

D. It does not accept asynchronous inputs

Ans.: A

40. A flip-flop is connected to +5 volts and it draws 5 mA of current during its operation, the power dissipation of the flip-flop is:

A. 10 mW **B. 25 mW** C. 64 mW D. 1024 mW

Ans.: B

41. _____ counters as the name indicates are not triggered simultaneously.

A. Asynchronous B. Synchronous

C. Positive-Edge triggered D. Negative-Edge triggered

Ans.: A

42. A synchronous decade counter will have _____ flip-flops.

A. 3 **B. 4** C. 7 D. 10

Ans.: B

43. A frequency counter _____.

A. Counts pulse width **B. Counts no. of clock pulses in 1 second**

C. Counts high and low range of given clock pulse D. None of given options

Ans.: B

44. The storage cell in SRAM is:

A. a flip –flop **B. a capacitor** C. a fuse D. a magnetic domain

Ans.: B

45. For a positive edge-triggered J-K flip-flop with both J and K HIGH, the outputs will_____ if the clock goes HIGH.

A. toggle B. Set C. reset D. not change

Ans.: A

46. If an S-R latch has a 1 on the S input and a 0 on the R input and then the S input goes to 0, the latch will be:

A. set B. reset C. invalid D. Clear

Ans.: A

47. The power dissipation (*P*D) of a logic gate is the product of the:

A. dc supply voltage and the peak current

B. dc supply voltage and the average supply current

C. ac supply voltage and the peak current

D.ac supply voltage and the average supply current

Ans.: A

48. The 3-variable Karnaugh Map (K-Map) has _____ cells for min or max terms.

A. 4 **B. 8** C. 12 D. 16

Ans.: B

49. Sum term (Max term) is implemented using _____ gates.

A. OR B. AND C. NOT D. OR-AND

Ans.: A

50. The output of an AND gate is one when _____.

A. **All of the inputs are one** B. Any of the input is one

C. Any of the input is zero D. All the inputs are zero

Ans.: A