Interfacing of memory and I/O:

1. The operation, $\overline{IOW}$ erforms
   A. write operation on input data B. write operation on output data
   C. read operation on input data D. read operation on output data
   Answer: B
2. If a typical static RAM cell require 6 transistors then corresponding dynamic RAM requires
   A. 1 transistor along with capacitance
   B. 2 transistors along with resistance
   C. 3 transistors along with diode
   D. 2 transistors along with capacitance
   Answer: A
3. If the size of a memory chip is 512 x 1 bits how many chips are required to make up 1 K bytes of memory?
   A. 2 B. 8 C. 16 D. 1024
   Answer: C
4. If the memory chip size is 1024 x 4-bits how many chips are required to make 4K bytes of memory?
   A. 4 B. 8 C. 16 D. 4096
   Answer: B
5. The synchronization between microprocessor and memory is done by
   A. ALE signal B. HOLD signal
   C. READY signal D. None of these
   Answer: C
6. For the most Static RAM the write pulse width should be at least
   A. 10ns B. 60ns C. 300ns D. 1μs
   Answer: B
7. SD RAM refers to
   A. Synchronous DRAM B. Static DRAM
   C. Semi DRAM D. Second DRAM
   Answer : (A)
8. Acess time is faster for
   A. ROM B. SRAM C. DRAM D. EPROM
   Answer: B
9. The no. of address lines required to address a memory of size 32 K is
   A. 15 lines B. 16 lines C. 18 lines D. 14 lines
   Answer: A

Programmable Input – Output 8255:

1. All the functions of the ports of 8255 are achieved by programming the bits of an internal register called
   A. data bus control B. read logic control
   C. control word register D. none
   Answer: C
2. When the 82C55 is reset, its I/O ports are all initializes as
   (A) output port using mode 0 (B) Input port using mode 1
   (C) output port using mode 1 (D) Input port using mode 0
   Answer: D
3. In 8255A _____ is used for input operation
   A. mode 0 B. mode2 C. mode 3 D. mode1
   Answer: A
4. In 8255A _____ is used for handshaking operation
   A. mode 0 B. mode1 C. mode 2 D. mode3
   Answer: B
5. In 8255 A _____ is used to perform bidirectional operation
   A. mode 0 B. mode1 C. mode 2 D. mode3
   Answer: C
6. Data transfer between the microprocessor for peripheral takes place through
   A. I/O port B. input port C. output port D. multi port
   Answer: A
7. In 8255A, there are _____ I/O lines
   A. 24 B. 12 C. 20 D. 10
   Answer: A
8. The 8255A is available with _____.
   A. 20 B. 40 C. 30 D. 10
   Answer: B
9. _____ is used to transfer data between microprocessor and I/o process
   A. 8255A B. 8279 C. 8254A D. 8237A
   Answer: A
10. 8255A contains_____ ports each of 8 bit lines
    A. 2 B. 4 C. 5 D. 3
    Answer: D
11. The _____ input to 8255 is usually activated by Microprocessor in system
    A. clear B. reset C. ports D. address bus
    Answer: B
12. The input provided by the microprocessor to the read/write control logic is
    A. RESET B. A_1 C. $\overline{WR}$ D. All of the above
    Answer: D

Communication Interface:

1. In 8251A, the pin that controls the rate at which the character is to be transmitted is
   A. $\overline{T_XC}$ B. T_XC C. $\overline{T_XD}$ D. R_XC
   Answer: A
2. T_XD(Transmitted Data Output) pin carries serial stream of the transmitted data bits along with
   A. start bit B. stop bit C. parity bit D. all of the above
   Answer: D
3. The signal that may be used either to interrupt the CPU or polled by the CPU is
   A. $T_X\overline{RDY}$(Transmitter ready) B. $R_X\overline{RDY}$(Receiver ready output)
   C. $\overline{DSR}$ D. $\overline{DTR}$ Answer: B
4. 8251 is a
   (A) UART (B) USART (C) Programmable Interrupt controller
   (D) Programmable interval timer/counter
   Answer: B
5. Which of the following is not a mode of data transmission?
   A. simplex B. duplex C. semi duplex D. half duplex
   Answer: C
6. If the data is transmitted only in one direction over a single communication channel, then it is of
   A. simplex mode B. duplex mode
   C. semi duplex mode D. half duplex mode
   Answer: A
7. In 8251 there are _____ pins
   A. 16 B. 24 C. 28 D. 40 Answer: C

8. The input clock frequency of 8251 is _____ times the T_XC or R_XC frequency
   A. 10 B. 15 C. 20 D. 30 Answer: D
9. The 8251 has,_____ 8 bit buffer used to interface internal data bus of to the system data bus.
   A. tri state bidirectional B. tri state unidirectional
   C. active unidirectional D. None of above
   Answer: A
10. The signals connected to MODEM section of 8251 USART are
    A. $\overline{DSR}$ &$\overline{DTR}$ B. $\overline{RTS}$ C. $\overline{CTS}$ D. All the above
    Answer: D

Programmable Interval Timer:

1. The number of counters that are present in the programmable timer device 8253 is
   A. 1 B. 2 C. 3 D. 4 Answer: C
2. The operation that can be performed on control word register in 8253 is
   A. read operation B. write operation
   C. read and write operations D. none Answer: D
3. The mode of 8253 that is used to interrupt the processor by setting a suitable terminal count is
   A. mode 0 B. mode 1 C. mode 2 D. mode 3
   Answer: A
4. The generation of square wave is possible using 8253 in the mode
   A. mode 1 B. mode 2 C. mode 3 D. mode 4
   Answer: C
6. In control word register of 8253, if SC1=0 and SC0=1, then the counter selected is
   A. counter 0 B. counter 1 C. counter 2 D. none
   Answer: B
7. The control word register contents of 8253 are used for
   A. initialising the operating modes B. selection of counters
   C. choosing binary/BCD counters D. all of the above
   Answer: D
8. 8253 chip is _____ chip.
   A. timer counter B. the interrupt controller.
   C. the DMA controller D. general-purpose parallel interface
   Answer: A
9. 8253 counter pin OUT is to _____. (A)
   A. indicates the counting process ends B. start counting process
   C. control counting process D. input clock signal
   Answer: A
10. The 8253 contains _____ counters
    A. 2-16 bit B. 3-16 bit C. 2-8 bit. D. 3-8 bit
    Answer: B
11. In 8253 there are _____ pins
    A. 20 B. 24 C. 30 D. 40 Answer: B
12. 8086 microprocessor is interfaced to 8253 a programmable interval timer. The maximum number by which the clock frequency on one of the timers is divided by
    a) 2^{16} b) 2^{8} c) 2^{10} d) 2^{20} Answer: A