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## MCQs on 8086 Microprocessor Sem.-VI

1. A microprocessor is a _____ chip integrating all the functions of a CPU of a computer

A. multiple **B. Single** C. double D. triple

2. Microprocessor is a/an _____ circuit that functions as the CPU of the compute

**A. Electronic** B. mechanic C. integrating D. processing

3. Microprocessor is the _____ of the computer and it perform all the computational tasks

A. main **B. Heart** C. important D. simple

4. The purpose of the microprocessor is to control _____

**A. Memory** B. switches C. processing D. tasks

5. The first digital electronic computer was built in the year_____

A. 1950 B. 1960 **C. 1940** D. 1930

6. In 1960's texas institute invented _____

**A. Integrated circuits** B. microprocessor C. vacuum tubes D. transistors

7. The intel 8086 microprocessor is a _____ processor

A. 8 bit **B. 16 bit** C. 32 bit D. 4 bit

8. The microprocessor can read/write 16 bit data from or to _____

**A. Memory** B. i/o device C. processor D. register

9. In 8086 microprocessor , the address bus is _____ bit wide

A. 12 bit B. 10 bit C. 16 bit **D. 26 bit**

10. The work of EU is _____

A. encoding **B. Decoding** C. processing D. calculations

11. The 16 bit flag of 8086 microprocessor is responsible to indicate _____

**A. The condition of result of ALU operation**
B. the condition of memory
C. the result of addition
D. the result of subtraction

12. The CF is known as _____

**A. Carry flag** B. condition flag C. common flag D. single flag

13. The SF is called as _____

A. service flag **B. Sign flag** C. single flag D. condition flag

14. The OF is called as _____

**A. Overflow flag** B. overdue flag C. one flag D. over flag

15. The IF is called as _____

A. initial flag B. indicate flag C. Interrupt flag D. inter flag

16. The register AX is formed by grouping _____

**A. AH & AL** B. BH & BL C. CH & CL D. DH & DL

17. The SP is indicated by _____

A. single pointer **B. Stack pointer** C. source pointer D. destination pointer

18. The BP is indicated by _____

**A. Base pointer** B. binary pointer C. bit pointer D. digital pointer

19. The SS is called as _____

A. single stack **B. Stack segment** C. sequence stack D. random stack

20. The index register are used to hold _____

**A. Memory register** B. offset address C. segment memory D. offset memory

21. The BIU contains FIFO register of size _____ bytes

A. 8 **B. 6** C. 4 D. 12

22. The BIU prefetches the instruction from memory and store them in _____

**A. Queue** B. register C. memory D. stack

23. The 1 MB byte of memory can be divided into _____ segment

A. 1 Kbyte **B. 64 Kbyte** C. 33 Kbyte D. 34 Kbyte

24. The DS is called as _____

**A. Data segment**
B. digital segment
C. divide segment
D. decode segme

25. The CS register stores instruction _____ in code segment

A. stream B. path **C. Codes** D. stream line

26. The IP is _____ bits in length

A. 8 bits B. 4 bits **C. 16 bits** D. 32 bits

27. The push source copies a word from source to _____

**A. Stack** B. memory C. register D. destination

28. LDs copies to consecutive words from memory to register and _____

A. ES **B. DS** C. SS D. CS

29. Inc destination increments the content of destination by _____

**A. 1** B. 2 C. 30 D. 41

30. IMUL source is a signed _____

**A. Multiplication** B. addition C. subtraction D. division

31. _____destination inverts each bit of destination

**A. NOT** B. NOR C. AND D. OR

32. The JS is called as _____

**A. Jump the signed bit** B. jump single bit C. jump simple bit
D. jump signal it

33. Instruction providing both segment base and offset address are called _____

A. below type **B. Far type** C. low type D. high type

34. The conditional branch instruction specify _____ for branching

**A. Conditions** B. instruction C. address D. memory

35. The microprocessor determines whether the specified condition exists or not by testing the _____

A. carry flag **B. Conditional flag** C. common flag D. sign flag

36. The LES copies to words from memory to register and _____

A. DS B. CS **C. ES** D. DS

37. The _____ translates a byte from one code to another code

**A. XLAT** B. XCHNG C. POP D. PUSH

38. The _____ contains an offset instead of actual address

A. SP **B. IP** C. ES D. SS

39. The 8086 fetches instruction one after another from _____ of memory

**A. Code segment** B. IP C. ES D. SS

40. The BIU contains FIFO register of size 6 bytes called _____

**A. Queue**
B. stack
C. segment
D. register

41. The _____ is required to synchronize the internal operands in the processor CIK Signal

**A. UR Signal** B. Vcc C. AIE D. Ground

42. The pin of minimum mode AD0-AD15 has _____ address

A. 16 bit **B. 20 bit** C. 32 bit D. 4 bit

43. The pin of minimum mode AD0- AD15 has _____ data bus

A. 4 bit B. 20 bit **C. 16 bit** D. 32 bit

44. The address bits are sent out on lines through _____

**A. A16-19** B. A0-17 C. D0-D17 D. C0-C17

45. _____ is used to write into memory

A. RD **B. WR** C. RD / WR D. Chk

46. The functions of Pins from 24 to 31 depend on the mode in which _____ is operating

A. 8085 **B. 8086** C. 80835 D. 80845

47. The RD,WR,M/IO is the heart of control for a _____ mode

**A. Minimum**
B. maximum
C. compatibility mode
D. control mode

48. In a minimum mode there is a _____ on the system bus

**A. Single**
B. double
C. multiple
D. triple

49. If MN/MX is low the 8086 operates in _____ mode

A. Minimum **B. Maximum** C. both (A) and (B) D. medium

50. In max mode, control bus signal So,S1 and S2 are sent out in _____ form

A. decoded **B. Encoded** C. shared D. un shared

51. The ___ bus controller device decodes the signals to produce the control bus signal

A. internal B. data **C. External** D. address

52. A _____ Instruction at the end of interrupt service program takes the execution back to the interrupted program

A. forward
**B. Return**
C. data
D. line

53. The main concerns of the _____ are to define a flexible set of commands

**A. Memory interface** B. peripheral interface C. both (A) and (B)
D. control interface

54. Primary function of memory interfacing is that the _____ should be able to read from and write into register

A. multiprocessor
**B. Microprocessor**
C. dual Processor
D. coprocessor

55. To perform any operations, the Mp should identify the _____

**A. Register**
B. memory
C. interface
D. system

56. The Microprocessor places _____ address on the address bus

A. 4 bit B. 8 bit **C. 16 bit** D. 32 bit

57. The Microprocessor places 16 bit address on the add lines from that address by _____ register should be selected

A. address **B. One** C. two D. three

58. The _____of the memory chip will identify and select the register for the EPROM

**A. Internal decoder** B. external decoder C. address decoder
D. data decoder

59. Microprocessor provides signal like ____ to indicate the read operation

A. LOW B. MCMW **C. MCMR** D. MCMWR

60. To interface memory with the microprocessor, connect register the lines of the address bus must be added to address lines of the _____ chip

A. single **B. Memory** C. multiple D. triple

61. The remaining address line of _____ bus is decoded to generate chip select signal

A. data **B. Address** C. control bus D. both (a) and (b)

62. _____ signal is generated by combining RD and WR signals with IO/M

**A. Control** B. memory C. register D. system

63. Memory is an integral part of a _____ system

A. supercomputer **B. Microcomputer** C. mini computer
D. mainframe computer

64. _____ has certain signal requirements write into and read from its registers

**A. Memory** B. register C. both (a) and (b) D. control

65. The memory chips such as 2732 EPROM and _____static R/W memory plays a major role in memory interfacing

A. 2732 EPROM **B. 6116** C. 8085 D. 8086

66. An _____ is used to fetch one address

**A. Internal decoder** B. external decoder C. encoder D. register

.

67. The primary function of the _____ is to accept data from I/P devices

A. multiprocessor
**B. Microprocessor**
C. peripherals
D. interfaces

68. Designing logic circuits and writing instructions to enable the microprocessor to ommunicate with peripheral is called _____

**A. Interfacing** B. monitoring C. polling D. pulling

69. _____ means at the same time, the transmitter and receiver are synchronized with the same clock.

A. asynchronous B. serial data **C. Synchronous** D. parallel data

70. _____ means at irregular internals

**A. Asynchronous** B. synchronous C. data transform D. bus transform

71. _____ signal prevent the microprocessor from reading the same data more than one

A. pipelining **B. Handshaking** C. controlling D. signaling

72. Bits in IRR interrupt are _____

A. reset **B. Set** C. stop D. start

73. _____ decides the request of interrupt to be serviced

**A. Priority resolver** B. interrupt request register C. interrupt mask register
D. control logic

74. _____ generate interrupt signal to microprocessor and receive acknowledge

A. priority resolver **B. Control logic** C. interrupt request register
D. interrupt register

75. The _____ is used to connect more microprocessor

A. peripheral device **B. Cascade** C. i/o deviced D. control unit

76. The 8259-A is a _____

**A. Piority Interrupt Controller** B. priority Resolver
C. interrupt Request Registry D. control Logic

77. The 8259A is used to manage _____ hardware in the system

A. Single **B. Multiple** C. Double D. none

78. _____ is used to transfer data between microprocessor and I/o process

**A. 8255A** B. 8279 C. 8254A D. 8237A

79. 8255A contains_____ ports each of 8 bit lines

A. 2 B. 4 C. 5 **D. 3**

80. In 8255A the ____ is controlled by control registers

A. port A B. port B **C. Port C** D. port D

81. _____ is used to transfer address connect to address block

A. data bus **B. Address bus** C. bus D. flag

82. _____ performs the address decode operation

**A. chip select** B. address bus C. data bus D. flag

83. Data transfer between the microprocessor for peripheral takes place through _____

**A. I/O port** B. input port C. output port D. multi port

91. The device such as buffer and batches are used as _____.

A. input port B. output port **C. I/O port** D. multi port

92. The pins are _____ data lines and are connected to data bus in system

A. unidirectional **B. Bidirectional** C. directional
D. multidirectional

93. _____ are transferred on the data lines between microprocessor and internal port or control register

**A. Data, control and status bites** B. data and status bits
C. control and status bites D. status bits

94. The address bus enables the _____ for data transfer.

**A. Control register** B. data bus C. address bus D. both (b) and (c)

95. The _____ are connected to 2 address bus line in system

A. address bus B. data bus **C. Pins** D. control bus

96. Smart Card on a microprocessor is for _____

A. safety **B. Security** C. protection D. authority

97. Smart card is used to provide _____

**A. Access** B. authority C. automation D. access control

98. Another name for smart card _____

**A. ICC** B. IFC C. IRC D. IC

99. Smart card is made up of _____

A. silicon B. iron **C. Plastic** D. rubber

100. The most common smart card application is _____.

**A. Credit card** B. atm card C. business card D. system card